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Architecture and Control of a DFLL for Fine-Grain DVFS in GALS Structures

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Abstract *— Fine-grain Dynamic Voltage and Frequency Scaling (DVFS) is becoming a requirement for Globally-Asynchronous Locally-Synchronous (GALS) architectures. However, the area overhead of adding voltage and frequency control engines in each voltage and frequency island must be taken into account to optimize the circuit. A small-area fast-reprogrammable Digital Frequency-Locked Loop (DFLL) engine is a suited option, since its implementation in 32nm represents 0.0016 mm², being 4 to 20 times smaller than classical used techniques such as Phase-Locked Loop (PLL) in the same technology. Another relevant aspect with respect to the DFLL is the control design, which must be suited for low area hardware. In this paper, an analytical model of the system is deduced from accurate Spice simulations. It takes into account the delay introduced by the sensor. From this model, an optimal and robust controller with a minimum implementation area is developed. The closed-loop system stability as well as the robustness against process and temperature variations are also ensured.*

Keywords — Frequency-Locked Loop (FLL), Digitally-Controlled Oscillator (DCO), robust control, optimization, system stability, perturbation rejection.

1 INTRODUCTION AND RELATED WORKS

The continuous increase in clock frequency together with technology scaling has generated the distribution of a single global clock over a large digital chip tremendously difficult. Globally Asynchronous Locally Synchronous (GALS) design alleviates the problem of clock distribution by having multiple clocks, each one being distributed on a small area of the chip. An integrated circuit with different clock frequency domains appears as a natural enabler for fine-grain power-aware architectures. Actually, power consumption is a limiting factor in VLSI integration, especially for mobile applications. Dynamic Voltage and Frequency Scaling (DVFS) [1] has proven to be highly effective to reduce the power consumption of the chip while meeting the performance requirements [2]. The key idea behind local DVFS is to control at fine grain the supply voltage and the frequency of an island at runtime to minimize the power consumption of the considered island while satisfying the computation/throughput constraints [3].

The DVFS techniques mainly rely on two ‘actuators’, namely voltage and frequency actuators. These actuators need to be dynamically controlled in order to reduce the power consumption while maintaining the required performance. More precisely, the control policy must be carefully designed in order to achieve high power efficiency at low area cost. The voltage actuator fixes the supply voltage of the Voltage and Frequency Island (VFI). It can be a classical buck converter [4] or a digital Vdd-hopping converter [5], [6]. The frequency actuator is a Clock Generator. Its frequency control is related to the supply voltage control in order to avoid timing faults [7]. This Clock Generator is classically based on a Phase-Locked Loop (PLL) or a Frequency-Locked Loop (FLL).

Another consequence of technology scaling is the in-die and die-to-die process variability (P-variability). From a practical viewpoint, it is becoming increasingly difficult to manufacture integrated circuits with tight parametric values [6]. In other words, the circuit performance is

becoming more and more unpredictable and the optimum functional frequency can differ from one IP to another on the same chip not only due to Process variation but also to Temperature and Voltage changes (PVT) over time. As a consequence, in-die process variation means that the optimum functional and energetic point of the whole circuit can be found if VFI number *i* has its functioning frequency in the range $[F_{\min,i}, F_{\max,i}]$ [8]. If the clock is generated for the whole circuit, and distributed in each VFI, the maximum acceptable frequency (i.e. the one that will ensure no timing fault for any VFI) will be $F_{\max} = \min\{F_{\max,i} \; \forall \; i\}$, leading to a suboptimal circuit functioning, some VFI being under-clocked. Therefore, in order to obtain the best possible circuit performance, the clock must be locally generated and controlled according to Process, Voltage and Temperature (PVT) variations. Recently, control techniques were applied to the problem of DVFS (for instance, see [5], [9]). These works only address the closed-loop control of the voltage actuator, this latter implementing a Vdd-hopping technique.

1.1 Structure of the closed-lopp system and main objectives

In the context of the industrial French project LoCoMoTiV[1] , a DFLL is selected as second actuator (i.e. frequency actuator) due to the area constraint: in a fine-grain GALS context, the DFLL can indeed be replicated in each VFI of the size of a processor in a manycore architecture. The frequency range at the FLL output is $[1, 4]$ GHz. The DFLL was implemented in 32nm technology. The layout developed is fully compatible with standard cell methodology, to be easily integrated at GALS System on Chip (SoC) level. Its area is about 0.0016 mm^2 which is 4 to 20 times smaller than a classical PLL in the same technology.

The first objective of the present paper is to propose a particular implementation for the *fully Digital FLL* (DFFL) that was integrated in each VFI of the LoCoMoTiV circuit. Note that this paper

[1] Local Compensation of Modern Technology Induced Variability (LoCoMoTiV) is a CEA-LETI Minatec Campus internal Project.

is not dedicated to LoCoMoTiV but to the design of the control law embedded in the DFLL that must be robust to PVT variability. The general structure of the DFLL (see Figure 1) is composed of three main blocks, namely, a Digitally-Controlled Oscillator (DCO) that provides at its output a signal with frequency *clk_dco*, a sensor to measure the frequency at the output of the closed-loop system, and a controller that first compares the targeted reference and the measured frequency and then applies some “intelligent control”. The controller design strongly depends on the DCO and sensor models. Due to PVT-variability, the characteristics of the DCO cannot be considered identical from one VFI of the chip to another, nor from one chip to another. Moreover, it evolves with temperature and power-supply voltage changes (VT-variability). Thus the closed-loop mechanism at least mitigates the performance dispersion. It is remarkable that the whole architecture is digital.

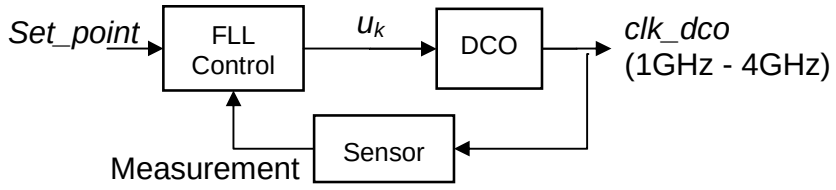

Figure 1. DFLL block diagram.

The second and main objective of the work presented in this paper is to design a controller for the DFLL taking into account the following requirements:

- closed-loop stability;
- suited performance (no overshoot, no static error, short transient period, see Figure 2);
- robustness with respect to PVT variations. The control law that will be implemented within the circuit must ensure the “correct” functioning of the DFLL whatever the underlying

process parameters, temperature and supply voltage are (within a given range);

- low area cost and
- exogenous perturbation rejection in the frequency output.

Therefore, the designed controller must not only guaranty the set-point stabilization, but also other criterions.

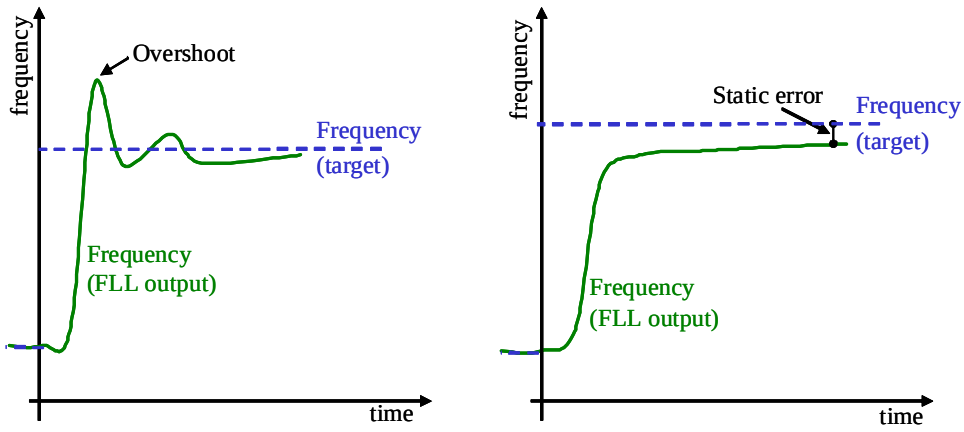

Figure 2. Overshoot of the frequency output not allowed.

From accurate Spice simulations, it has been seen that the DCO can be modeled with a linear model. Moreover, the sensor introduces a delay that must be taken into account. The system characteristic can change due to PVT effects. A simple integral controller that requires a minimum implementation area is enough to fulfill all the requirements given above. To tune the control gain, a robust and optimal control problem is formulated, for which a functional must be minimized. In order to solve this problem some Linear Matrix Inequalities (LMIs) are defined [11]. Satisfying these LMIs within the optimal problem, all requirements above are fulfilled by the closed-loop system. Consequently, an optimal and robust control law for the DFLL is reached.

Some simulations under the Matlab/Simulink environment show the powerfulness of the controller

proposed. Moreover, the closed-loop system was implemented in RTL, obtaining similar simulation results to the ones obtained in Matlab/Simulink. The resulting layout was implemented in the LoCoMoTiV circuit in CMOS 32nm.

1.2 Related Works

PLL or FLL circuits can be considered good candidates for frequency generation within integrated circuits. Both circuits are widely used building blocks. However, new or improved architectures still continue to appear in order to meet today constraints induced by technology scaling. PLLs are usually considered area consuming [12], which becomes clearly a disadvantage when the PLL has to be replicated in each VFI. Note that the stability of the PLL is also usually much more difficult to obtain than with an FLL. This is due to the "integrator" that naturally appears in the PLL structure.

A fully integrated PLL for frequency synthesis in wireless applications with 45nm CMOS technology is proposed in [13]. The analog PLL is made of a top-biased VCO, a divider in the feedback loop, a Phase/Frequency detector (PFD) and a charge pump. The output frequency ranges from 2 to 2.6 GHz. The loop filter is not explicitly reported. The area cost (0.042 mm²) of this analog PLL is slightly larger than the one (0.028 mm²) of an all-digital PLL developed in the same technology [8]. This latter digital PLL contains a DCO made with tri-state inverters, a digital Proportional-Integral (PI) controller and a divider in the feedback loop. The comparison between the reference frequency and the divided output frequency is achieved with a bang-bang phase/frequency detector (see [15] for a high level architecture scheme of the digital PLL). The output frequency range is from 0.84 to 13.3 GHz.

[16] describes a PLL with leakage current and power supply noise compensation, designed for 32nm technology. The PLL contains classical elements such as a PFD, a charge pump, a controller, a Voltage Controlled Oscillator (VCO, made of a cascade self-biasing current source and a current

starved ring oscillator with 11-stage of inverters) and a frequency divider, but also a leakage compensator, a Power Supply Noise Compensator (PSNC) and a voltage buffer block in the controller. The controller is a classical filtered PID. The output frequency ranges from 40 to 725 MHz. Results are obtained in simulation and no information on the area cost is given.

The FLL in [12] is made of two Frequency-to-Voltage Converters (FVC), an operational amplifier (equivalent to a subtractor and a simple proportional filter), a VCO (ring oscillator of five delay cells) and two frequency dividers. Note that both FVC must be carefully paired to reduce the static error. However, due to the control scheme chosen, the static error is unavoidable. Therefore, this scheme will not be able to fulfill the requirements given above. With 0.35µm CMOS technology, the total active area of the circuit is 0.22 mm². The response time to switch the output frequency from 171 to 230 MHz is 2 µs. The VCO output frequency ranges from 161 MHz to 256 MHz.

A digital FLL for low power operation in multicore architecture is described in [17]. The targeted application is quite similar to the one of the present work. A tapped ring oscillator is implemented. A digital counter senses the FLL output frequency. A compare-subtract bock computes the discrepancy between the targeted set point and the frequency measurement. The input of the tapped ring oscillator is changed through a shift register when this discrepancy is lower/higher than a given threshold. The range of frequencies is between 1.62 and 10.71 GHz. The estimated size is 0.001225 mm². Note that the correlation between the frequency discrepancy and the shift is not indicated and the control cannot be strictly speaking considered as a classical control scheme. Results are obtained in simulation with IBM soi12s0 technology (45nm).

[18] describes a dual-loop Clock and Data Recovery circuit with frequency-aided acquisition to enhance the tracking range. The FLL and PLL activate alternatively. The closed-loop system contains a special phase detector, a charge pump, a controller and a VCO built with a voltage/current block

and a Current-Controlled Oscillator (ICO). The open-loop transfer function is of 3rd order with a double integrator and a filtered Proportional-Derivative filter as controller. Note that due to this double integrator, any uncertainty in the capacitor values of the controller will induce stability concerns, not acceptable for a safe functioning of the closed loop system. The circuit has been fabricated in 0.35µm technology.

As can be seen, to our knowledge, none of the previously published systems fully satisfy the requirements that have been fixed for this circuit design. Therefore, a *Fully Digital variability-aware DFLL* is developed.

Table I summarizes the characteristics of the frequency generation circuits summarized above.

TABLE I
COMPARISON OF FREQUENCY GENERATION CIRCUITS ("-" MEANS "MISSING INFORMATION")

Ref.	Type	Tech. nm	Output Freq.	Area mm²	Resp. time
[13]	Analog PLL	45	-	0.042	-
[14]	Digital PLL	45	[0.84; 13.3] GHz	0.028	-
[16]	PLL	32	[40; 725] MHz	-	-
[12]	FLL	350	[161; 256] MHz	0.22	2 µs
[17]	Digital FLL	45	[1.62; 10.71] GHz	0.001225	-
[18]	Dual digital FLL-PLL	350	1.25 GHz	-	-

The rest of the paper is organized as follows. Section 2 provides the architecture of the blocks that form the DFLL. The analytical models of the DFLL blocks are presented in Section 3. Section 4 is dedicated to the control structure that is selected here, and an optimal and robust control problem is also formulated. In Section 5, this problem is solved by providing an approach to tune the controller gain. The results obtained together with a comparison with state-of-the-art solutions are provided in Section 6. The paper ends with conclusions and future work.

1.3 Notation

For a given *S*, the notation *Co(S)* denotes the convex hull of set *S*. The variation of ξ in two consecutive sampling times is given by:

$$\Delta\xi := \xi_{k+1} - \xi_k \qquad (1)$$

Finally, L_2 is the space of x_k with the norm:

$$\|x_k\|_2^2 := \sum_{k=0}^{\infty} x_k^T x_k < \infty \qquad (2)$$

2 DFLL ARCHITECTURE

In order to model and develop the DFLL control, the architecture that implements the DFLL is analyzed in this section. A classic closed-loop DFLL is composed of three main blocks: a DCO, a sensor and a controller (see Figure 1). However, for implementation issues, the whole DFLL is split in five main elements (see Figure 3):

- the **Digitally-Controlled Oscillator (DCO)** is composed of a Digital-to-Analog Converter (DAC) and a Voltage-Controlled Oscillator (VCO);
- the **DFLL Control** implements the controller and handles the configuration from the host;
- the **Clock Counter** acts as sensor. It measures the clock generated by the DCO;
- the **Clk-ref Counter** generates the time reference signals;
- the **Clk Divider & Selector** builds various divider clocks and selects the appropriate one to obtain the output clock *clk_out*.

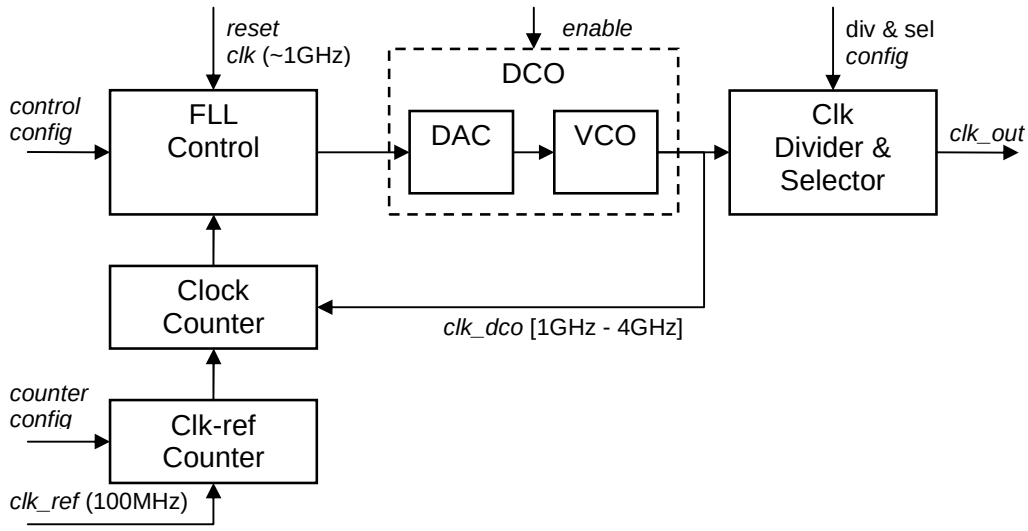

Figure 3. DFLL architecture.

2.1 Digitally-Controlled Oscillator

The DCO is the only part of the design that is implemented in custom cells. The VCO (Figure 4) is based on a ring oscillator composed of four Voltage Controlled Delay cells (VCD) [19]. The propagation delay through these delay cells is controlled by two bias voltages, namely, an upper bias and a lower bias. To obtain the DCO, a binary code (F_{req}) is transformed by two R-2R DACs into an upper and a lower bias voltage applied to the VCO. The two DACs are composed of driving buffers (simple digital standard cells) and a resistance ladder following an R-2R pattern. The DAC output impedance *R* is set to drive the VCO input.

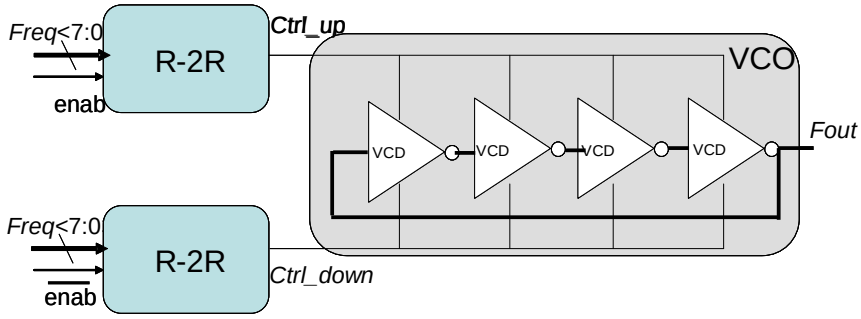

Figure 4. DCO architecture.

Overall, the linearity of such circuit is affected by stochastic resistance variability, but the absence of any analog amplification (no analog buffer or OTA) makes the design extremely compact and more robust. Figure 5 shows the frequency characteristics of the post-layout DCO (with extracted *R* & *C* parasites) in function of the 8-bits binary word input. The Y-axis corresponds to the measured raw frequency: this frequency must be divided by 2 to obtain a usable clock frequency with a 50% duty ratio. The "nominal" case (curve in the middle) is measured at 25°C with a 1.1 V supply voltage. The "best" case (top curve) is obtained with best case parasitic extract (minimum *R*, minimum *C*), 'FastFast' transistors, with supply voltage of 1.2 V and a temperature of 125°C. The "worst" case simulation is performed with worst case parasitic extract (maximum *R*, maximum *C*), 'SlowSlow' transistors, at 1.0 V supply voltage and a temperature of 0°C. This figure shows also the nominal output frequency, which corresponds to 4 GHz for the maximum input.

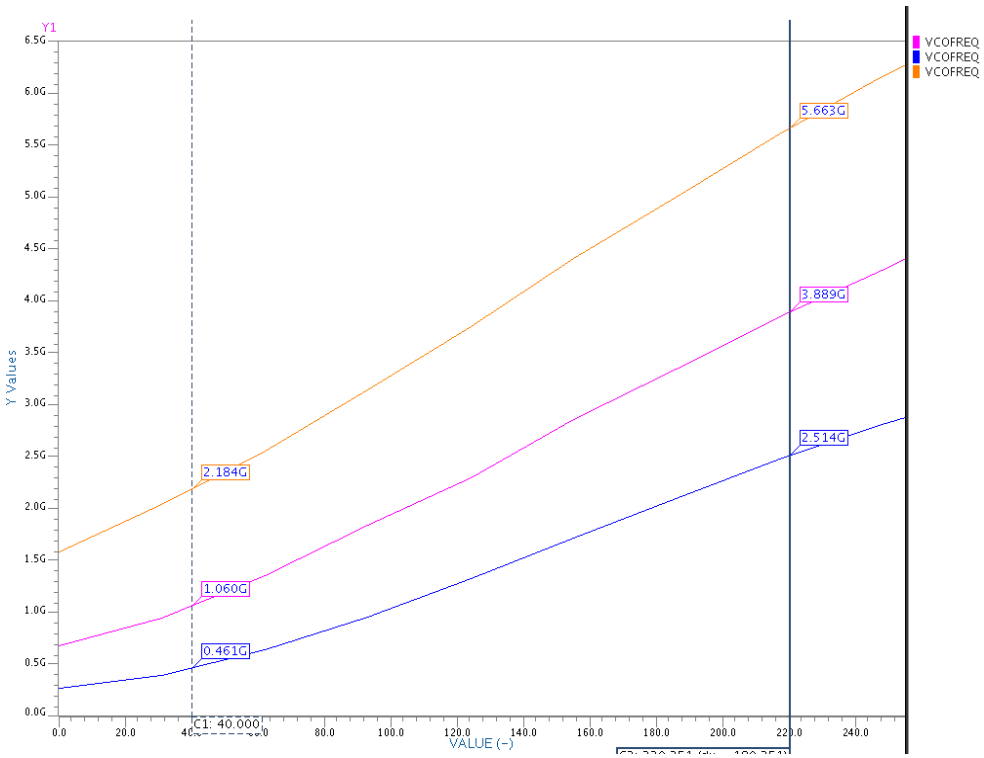

Figure 5. DCO characteristic (Measured raw frequency vs. input word).

2.2 Sensor

The feedback sensor is implemented as a synchronous counter. This device counts the number of generated clock pulses during a given time period. This reference time is fixed and synchronized with an external low frequency clock (100 MHz). In the proposed architecture (see Figure 3), the sensor is implemented by the two blocks Clock Counter and Clk-ref Counter.

The Clk-ref Counter generates two reference control signals from the external low frequency clock, which are the *count* and *update* signals. The *count* signal indicates the count period while the *update* signal indicates when the measurement should be read by the Clock Counter. The count period is programmable between 1 and 7 reference clock periods. The Clk-ref Counter is implemented as a controlled synchronous counter, clocked on *clk_ref* at 100 MHz. For the nominal case (maximum output 4 GHz, see Figure 5), the count period is 5 reference clock periods.

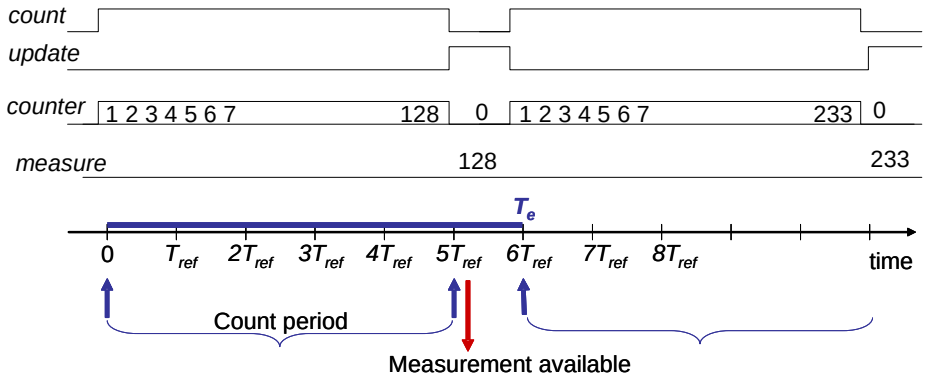

Figure 6. Synchronous counter: counting chronogram. Here the sampling period is $T_e = 6T_{ref}$.

The Clock Counter acts as the real sensor, counting the number of pulses generated by the DCO. It is implemented as an asynchronous ripple counter controlled by the *count* and *update* signals generated by the Clk-ref Counter. Once the *update* phase starts, the counter is registered to be used by the DFLL Control engine, and the counter is cleared to start the next *count* phase. Figure 6 shows the

counting chronogram. Note that for 5 reference clock periods the total sensor delay corresponds to 60 ns.

The Clock Counter is fully implemented using the *clk_dco* domain. Since this counter needs to be very fast, the counter is partially conceived as an asynchronous ripple counter. The 2 first bits are implemented as a ripple counter; this decreases the maximum input frequency *clk_dco* from 4 GHz (in the nominal case) down to 2 GHz (for bit 0) and down to 1 GHz (for bit 1). Then a standard incrementer is used, at 1 GHz, instead of a full carry ripple adder, avoiding a large skew in the output bits (see Figure 7). The two input control signals, *count* and *update* (generated from the *clk_ref* domain), need to be properly synchronized with *clk_dco*. A schematic view of the Clock Counter is presented in Figure 7.

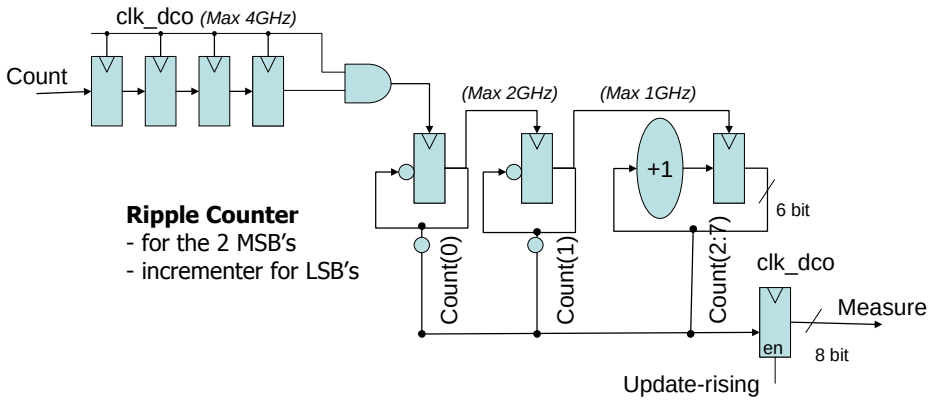

Figure 7. Counter schematic.

2.3 Controller

The controller implemented in this architecture will ensure the proper functioning of the circuit. It is designed not only for the closed-loop system to reach the set point, but also to fulfill the requirements given in Section 1.1. The controller proposed is described in details in Section 4 while the method used to tune its parameter is given in Section 5.

This controller must be developed taking into account its hardware implementation and the area constraint.

2.4 Clock Divider and Selector

The frequency of the DCO output signal is in the range 1 to 4 GHz. This high frequency cannot be directly used by digital synchronous circuits for the applications targeted. It is thus required to downscale the frequency generated in the MHz range. As a consequence, the following functions are provided:

- a clock division by a 21 to 216 ratio. This is simply implemented by chained flip-flops. The first flip-flop ensures a clean 50% duty-cycle at the DFLL output. The generated DFLL clock can therefore be from 2 GHz down to 100 KHz;

- a clock selector, which allows dynamically selecting among 2 clock division factors, without any glitches. This mechanism can be used to very rapidly switch between two frequencies. This can be used for instance for DVFS in coordination with Vdd-Hopping [6].

3 ANALYTICAL MODELS

The analytical models for the DFLL blocks (DCO and sensor as shown Figure 1) are derived in this section. These models will be used in order to choose the controller structure, taking into account the requirements given in Section 1.1.

3.1 Digitally-Controlled Oscillator

From accurate Spice simulations, it can be assumed that the DCO has a linear model that evolves with respect to Process variation but also to Temperature and Voltage changes (PVT) over time.

The DCO model is assumed be

$$clk\_dco_k = b + K_{dco}u_k + B_w w_k \quad (3)$$

$clk\_dco_k \in \Re^1$ is the analog frequency output, $u_k \in \aleph$ is coded over 8 bits between 0 and 255, respectively. b is the DC-offset, K_{DCO} is a gain. w_k is an energy-bounded signal to take account perturbations, and B_w is a constant that defines the perturbation magnitude. In order to consider the PVT variation effects, it is assumed that parameters K_{DCO}, b and B_w can change in the intervals

- $K_{DCO} \in [K_{DCO}^m, K_{DCO}^M]$
- $B_w \in [B_w^m, B_w^M]$
- $b \in [b^m, b^M]$

3.2 Sensor model

The sensor, which is a counter, measures the frequency of the DCO output signal. This sensor introduces a delay of one-sampling period

$$M_k := K_s \cdot clk\_dco_{k-1} \quad (4)$$

K_s is a positive constant that represents the sensor gain. Note that the delay is present in the feedback loop, see Figure 1.

4 CONTROLLER STRUCTURE AND CONTROL PROBLEM STATEMENT

4.1 Structure of the controller

From the requirements provided in Section 1 and the models of the DCO and the sensor, the DFLL control engine can be selected as a simple digital integral filter:

$$\frac{u(z)}{\varepsilon(z)} = K\frac{z}{z-1} \qquad (5)$$

where K is the controller gain to be tuned, u is the input of the DCO (see Figure 1) and ε is the difference between the *Set_point* (i.e. the desired output, coded on a byte) and the measurement M_k given in (4)

$$\varepsilon_k := K_s \cdot Set\_point - M_k \qquad (6)$$

Then, (5) yields

$$u_k = u_{k-1} + K \cdot (K_s Set\_point - M_k) = u_{k-1} + K\varepsilon_k \qquad (7)$$

Note that the choice of (7) for the controller structure will also limit the Silicon area.

The structure used to implement the controller is made of three arithmetic operators and a command register as shown in Figure 8. The first operator (*Sum0*) calculates the difference between the desired output (*Set_point*) and the measurement from the counter *M*, representing the frequency of the DFLL output signal. This error ε_k is affected by the controller gain K in the *Product* operator. Finally, the last addition (*Sum1*) and the register (Reg) implement the Backward Euler accumulator, being u_k the actual output applied to the DCO and u_{k-1} the output at the previous sampling time.

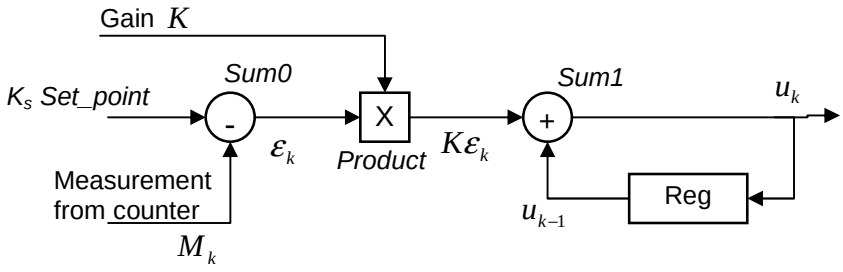

Figure 8. DFLL control engine.

The internal command value register (Reg) is updated each time the *clk_ref* generates a new update

signal, for instance every 6 *clk_ref* cycles in the present work. This means that a new control value u_k is computed from to the newly measured counter value M_k and from the previous control value u_{k-1} every 6 *clk_ref* values.

The whole data-path logic is implemented using only combinational logic. This logic clearly cannot be executed in only one cycle with a 1 GHz clock. Thus a multi-cycle path and its associated control logic is used. Note that they are not shown in Figure 8 for the sake of clarity. Finally, u_k is registered, to generate a stable value, to be sent out to the DCO.

The controller gain K must be selected in such a way that the closed-loop system satisfies the whole set of requirements.

4.2 Closed-loop system

Define the output error signal with

$$e_k := K_s \cdot Set\_point - clk\_dco_k \qquad (8)$$

Then, from (7), it comes that $u_k = u_{k-1} + KK_s e_{k-1}$.

An analytical closed-loop system is obtained. From (3) and (8), the error equation is

$$e_k = -b - K_{DCO} u_k - B_w w_k + K_s Set\_point \qquad (9)$$

Now, from (9) it follows that

$$u_{k-1} = \frac{-b - e_{k-1} - B_w w_{k-1} + K_s Set\_point}{K_{DCO}} \qquad (10)$$

Applying (10) in (8), it comes that

$$u_k = \frac{-b - e_{k-1} - B_w w_{k-1} + K_s Set\_point}{K_{DCO}} + KK_s e_{k-1} \qquad (11)$$

Then, the control law in (11) is introduced in the open-loop system (9), leading to the closed-loop system

$$e_k = e_{k-1} - K_{DCO}K_s K e_{k-1} + B_w w_{k-1} - B_w w_k \tag{12}$$

This can be rewritten in the following linear form:

$$e_{k+1} = Ae_k + B\bar{u}_{k+1} + B_w w_k - B_w w_{k+1}, \tag{13}$$

where

$$A = 1, \quad B = -K_{DCO}K_s \tag{14}$$

and

$$\bar{u}_{k+1} = Ke_k \tag{15}$$

Note that *b* does not influence the system response.

4.3 Control problem statement

Equation (12) can be rewritten in the following explicit closed-loop form, in such a way that a H_∞ control problem can be formulated:

$$e_{k+1} = Ae_k + B\bar{u}_{k+1} + B_w w_k - B_w w_{k+1} \tag{16}$$

$$z_{k+1} = e_{k+1} \tag{17}$$

Problem 1: The problem is to find the optimal gain *K*, such that the controller (7) is robust and the system response is the shortest possible without producing an overshoot. Besides, there exists a Lyapunov functional $V_k > 0$ such that $V_{k+1} - V_k$ along the solution of (16) fulfills

$$V_{k+1} - V_k < 0 \tag{18}$$

and for any perturbation input, there exists a minimum disturbance attenuation $\gamma^* \geq 0$ such that, for

all $\gamma \geq \gamma^*$, the L_2 gain between the perturbation vectors w_k and w_{k+1}, and the output vector z_{k+1} is less or equal to γ, i.e.

$$\|z_{k+1}\|_2^2 := \gamma(\|w_k\|_2^2 + \|w_{k+1}\|_2^2) < 0, \quad \forall w_k, w_{k+1} \in L_2 \tag{19}$$

The solution to this problem guarantees a suited performance as well as a robust stability and a robust disturbance rejection for system (16)-(17). Section 5 solves Problem 1 with an optimal H_∞ design of the controller.

5 OPTIMAL H_∞ CONTROL DESIGN

In order to cope with Problem 1, a mathematical manipulation of (16) is performed via a variable change. This allows obtaining feasible LMIs for a robustness problem [20].

5.1 Model transformation

Consider

$$y_k := e_{k+1} - e_k \tag{20}$$

Then, (16) is rewritten in the form [21]:

$$\begin{bmatrix} e_{k+1} \\ 0 \end{bmatrix} = \begin{bmatrix} y_k + e_k \\ -y_k + Ae_k - e_k + BKe_k + B_w w_k - B_w w_{k+1} \end{bmatrix} \tag{21}$$

This system can be compactly written as:

$$E\bar{e}_{k+1} = \bar{A}\bar{e}_k + \begin{bmatrix} 0 \\ B_w \end{bmatrix} w_k - \begin{bmatrix} 0 \\ B_w \end{bmatrix} w_{k+1} \tag{22}$$

where

$$\bar{A} = \begin{bmatrix} 1 & 1 \\ A + BK - 1 & -1 \end{bmatrix},$$
$$E := diag\{1,0\}, \quad \bar{e}_k := \begin{bmatrix} e_k \\ y_k \end{bmatrix}. \tag{23}$$

5.2 Control design

Problem 1 will be formulated in terms of Linear Matrix Inequalities (LMIs) [22].

Assumption 1: There exists a Lyapunov function V_k, with condition (18) and a γ, such that

$$V_{k+1} - V_k + z_{k+1}^T z_{k+1} - \gamma^2 (w_{k1}^T w_{k+1} + w_{k+1}^T w_{k+1}) \le \zeta^T \Gamma \zeta < 0 \tag{24}$$

where $\zeta := [\bar{e}_k \; w_k \; w_{k+1}]^T$ is an augmented state vector and $\Gamma \in \Re^{4\times4}$ is a symmetric matrix.

V_k is defined by the Lyapunov function

$$V_k = \bar{e}_k^T EPE\bar{e}_k, \tag{25}$$

where $P = \begin{bmatrix} P_1 & P_2 \\ P_2^T & 0 \end{bmatrix} \in \Re^{2\times2}$, $P_2 \neq 0$ and $P_1 > 0$.

Hereafter, a sufficient condition for asymptotic stability and disturbance rejection is derived.

Theorem 1: Consider system (16)-(17) with $K \in \Re^{1\times1}$ and energy-bounded w_k and w_{k+1}. If the following LMI is satisfied:

$$P_1 > 0$$
$$\Gamma := \begin{bmatrix} \bar{A}^T P \bar{A} - EPE + diag\{1,0\} & \bar{A}^T P \begin{bmatrix} 0 \\ B_w \end{bmatrix} & -\bar{A}^T P \begin{bmatrix} 0 \\ B_w \end{bmatrix} \\ * & -\gamma^2 & 0 \\ * & * & -\gamma^2 \end{bmatrix} < 0, \tag{26}$$

then the equilibrium of the closed-loop system (16)-(17) is asymptotically stable and there exists γ^*,

such that for $\gamma < \gamma^*$, condition (19) is fulfilled.

Proof: The goal is to satisfy (24) for both disturbance rejection and asymptotic stability of the equilibrium for system (16)-(17).

Lyapunov method yields:

$$\begin{aligned} V_{k+1} - V_k &= \bar{e}_{k+1}^T EPE\bar{e}_{k+1} - \bar{e}_k^T EPE\bar{e}_k = \left\{\bar{e}_k^T \bar{A}^T + w_k \lfloor 0\ B_w^T \rfloor - w_k \lfloor 0\ B_{w+1}^T \rfloor\right\} - \bar{e}_k^T EPE\bar{e}_k \\ &= \bar{e}_k^T [\ \bar{A}^T P\bar{A} - EPE\ ]\bar{e}_k + \bar{e}_k^T \bar{A}^T P\begin{bmatrix} 0 \\ B_w \end{bmatrix} w_k - \bar{e}_k^T \bar{A}^T P\begin{bmatrix} 0 \\ B_w \end{bmatrix} w_{k-1} \\ &+ w_k [0\ B_w^T\ ] P\bar{A}\bar{e}_k - w_{k+1} [0\ B_w^T\ ] P\bar{A}\bar{e}_k , \end{aligned} \tag{27}$$

The expression of $V_{k+1} - V_k$ in (24) is replaced by (27) in such a way that the LMIs (26) are obtained. □

5.3 Robust control

Now, the uncertain parameters given in Section 3 are taken into account in order to guarantee the system robustness at the same time than the closed-loop stability as well as disturbance rejection for the DFLL system to be ensured. This means that a robust control under parameter uncertainties satisfies those properties. For this reason, Theorem 1 is extended in the case of polytopic uncertainties.

Denote

$$\Omega = \begin{bmatrix} BK & B_w \end{bmatrix} \tag{28}$$

Assume that $\Omega \in Co\{\Omega_j, \quad j = 1,2,3,4\}$ namely

$$\Omega = \sum_{j=1}^{n} \lambda_j \Omega_j , \quad \text{for some} \quad 0 \le \lambda_j \le 1, \quad \sum_{j=1}^{n} \lambda_j = 1 \tag{29}$$

being the vertices of the polytope described by $\Omega_j = \begin{bmatrix} B^{(j)}K & B_w^{(j)} \end{bmatrix}$ for *j=1,2,3,4.*

Pre- and post-multiplying the LMI (26) by $Q = diag\{Q_1, Q_1, 1, 1\}$ and taking $Q_1 = P_2^{-1} > 0$ and $\overline{P}_1 = Q_1 P_1 Q_1$ the following sufficient condition is achieved.

Theorem 2: Consider system (16)-(17) with energy-bounded w_k and w_{k+1}, and $K \in \Re^{1\times 1}$. If there exist $T \in \Re^{1\times 1}$ with $K = TQ_1^{-1}$ such that

$$\overline{P}_1 > 0$$

$$\overline{\Gamma}^{(j)} := \begin{bmatrix} 2Q_1(A-1) + 2B^{(j)}T + 1 & \overline{P}_1 + Q_1(A-2) + TB^{(j)} & B_w^{(j)}Q_1 & -B_w^{(j)}Q_1 \\ * & \overline{P}_1 - 2Q_1 & B_w^{(j)}Q_1 & -B_w^{(j)}Q_1 \\ * & * & -\gamma^2 & 0 \\ * & * & * & -\gamma^2 \end{bmatrix} < 0, \; j = 1,2,3,4. \tag{30}$$

Then, in the vertices *j*, the equilibrium is asymptotically stable as well as the disturbances are rejected in the entire polytope.

Proof: This is an extension of Theorem 1 for polytopic uncertainties with some mathematical manipulations. Therefore, this theorem proof is straightforward. □

5.4 Optimal and robust control

In order to satisfy the whole Problem 1, more assumptions and a lemma are performed.

Assumption 2: For $w_k \equiv 0$ and $w_{k+1} \equiv 0$, the poles of the closed-loop system (16) are

$$Z = 1 + BK, \tag{31}$$

If $Z > 0$ is chosen, overshoots are avoided. In addition, if *K* is maximized, the response time is the shortest possible one [23]. Note that, $u_k = u_{k-1} + KK_s e_{k-1}$.

Remark 1: From Theorem 2, it is ensured that *Z<1*, that is, the closed-loop system is stable.

Assumption 3: There exists a functional cost

$$J := \|u_{k+1}\|_2^2 + \|z_{k+1}\|_2^2 - \gamma(\|w_k\|_2^2 + \|w_{k+1}\|_2^2) \tag{32}$$

The first term on the right hand side quantifies the response time. Likewise, the other terms (on the right hand side) quantify the perturbation attenuation.

Lemma 1: Suppose that Assumptions 1, 2 and 3 are fulfilled and $\overline{Z}^{(i)} = Q_1^T Z^{(j)} Q_1$. Then the optimal controller gain *K* for Problem 1 can be found by:

$$\begin{aligned} & K = \arg\min(-J) \\ & subject\ \ to: \\ & \qquad \overline{P}_1 > 0 \\ & \qquad \overline{\Gamma}^{(j)} < 0 \quad j = 1,2,3,4 \\ & \qquad \overline{Z}^{(i)} > 0 \quad i = 1,2 \end{aligned} \tag{33}$$

where

$$\overline{Z}^{(i)} = Q_1 + B^{(i)} \quad i = 1,2. \tag{34}$$

Proof: The optimal Problem 1 is solved by Lemma 1 if condition (19) is fulfilled [24]. □

For $w_k \neq 0$ and $w_{k+1} \neq 0$, and under zero initial conditions

$$V_{k+1} - V_k \leq -z_{k+1}^T z_{k+1} + \gamma^2 (w_k^T w_k + w_{k+1}^T w_{k+1}). \tag{35}$$

The sum of both sides is

$$V_{k+1} - V_k \leq -\sum_{k=0}^{k} z_{k+1}^T z_{k+1} + \gamma^2 \sum_{k=0}^{k} w_k^T w_k + \gamma^2 \sum_{k=0}^{k} w_{k+1}^T w_{k+1}. \tag{36}$$

For $k \to \infty$, under the zero initial condition $V_0 = 0$ and the positive definitiveness of the Lyapunov function, it is proved that

$$\sum_{k=0}^{\infty} z_{k+1}^T z_{k+1} \leq \gamma^2 \sum_{k=0}^{\infty} w_k^T w_k + \gamma^2 \sum_{k=0}^{\infty} w_{k+1}^T w_{k+1}. \tag{37}$$

$$\|z_{k+1}\|_2^2 \le \gamma(\|w_k\|_2^2 + \|w_{k+1}\|_2^2). \quad (38)$$

Corollary 1: The optimal gain *K* obtained applying Lemma 1 guaranties both robust stability and robust disturbance rejection. It also provides a short transient period without overshoots.

5.5 Optimal and robust control result

Now, an optimal and robust control is computed for the DFLL by employing the approach presented above.

Digitally-Controlled Oscillator. The DCO parameters can change within the following intervals:

$$K_{DCO} \in [10,30] \cdot 10^{-3} \text{ GHz / LSB} \quad (39)$$

The perturbation parameter is given by

$$B_w \in [0.1, \quad 0.4] \quad (40)$$

Sensor. The maximum frequency at the input of the sensor is supposed equal to 5GHz and $K_s = 85\,\text{LSB/GHz}$.

The optimal control problem (Problem 1) is solved leading to

$$K = 0.392, \quad (41)$$

together with $\gamma = 1.8$, and $P_1 = 0.2663$.

6 DFLL IMPLEMENTATION

This section deals with implementation issues of the DFLL. Firstly, the design and validation flow

is detailed. Then, Matlab/Simulink simulation results are discussed. Finally, the RTL design and experimental results are presented.

6.1 Design and validation flow

At the first stage of the design-flow, a full custom design has been performed for the DCO, validated at Spice level. It was characterized at various PVT corners, obtaining the results shown in Figure 5. Based on these results, a Matlab/Simulink model has been adjusted to describe the DCO functioning. The DFLL control architecture was then designed and tested in Matlab/Simulink applying the methodology proposed in Section 5. The Matlab/Simulink testbench was used to perform a fixed-point analysis of the data-path logic in order to optimize the precision and the area overhead.

Then, the implementation was done following the standard RTL methodology: the complete DFLL design has been developed in VHDL RTL. For validation proposes, a DCO behavior model has been given in VHDL in order to model the unique custom block of the system. A specific RTL test-bench has been developed to validate the DFLL behavior and the programming interfaces.

At the third design-flow level, specific Matlab/Simulink-RTL co-simulations have been performed between the RTL DFLL control parts and the Matlab/Simulink model of the DCO. These simulations validated the dynamic response and convergence of the real RTL design with the accurate DCO Matlab/Simulink model that has been identified from Spice simulation results at the first design-flow level.

The last design-flow level can be realized: synthesis and place&route using CMOS 32nm standard cells were performed with standard tools, considering the DCO as an analog macro. Post layout simulations on back-annotated Verilog netlist validated the placed and routed design and verified the correct timing constraints of the fast clock domains.

6.2 Matlab/Simulink simulations

Simulations in the Matlab/Simulink environment have been performed in such a way that the main model features were tested. A fixed-point analysis has been accomplished to determine the number of bits and point position needed for each operator and operand of the controller. The *Set_point* input as well as the gain input were fixed to unsigned 8 bits allowing a frequency precision of 20 MHz/LSB without clock division. Internal nodes were set as follows: $_{k-1}$ to signed 9 bits, K_{k-1} to signed 17 bits and fixed point at 8, u_k and u_{k-1} to unsigned 16 bits and fixed point at 8. u_k is resized to unsigned 8 bits prior its application to the DCO input since the DAC input is 8 bits. This bit sizing ensures that u_k can neither be negative nor greater than the DCO input range.

Hereafter, some simulations show the robustness of the controller proposed for the DFLL. The sampling period is equal 60 ns.

Remind that the DFLL characteristic curve can change due to PVT variations as shown in Figure 5. In order to validate the system robustness with respect to these changes, three different models are considered (see Figure 9):

- **syst 1:** $K_{DCO} = 19.8287 \cdot 10^{-3}$ and $b = -0.0315$;
- **syst 2:** $K_{DCO} = 14.25 \cdot 10^{-3}$ and $b = 4.5785$;
- **syst 3:** $K_{DCO} = 25.5 \cdot 10^{-3}$ and $b = 2.0785$.

The optimal and robust control gain has been fixed with the methodology presented in section 5. Therefore, whatever the characteristic of the DCO is, the closed-loop system will behave as expected. Moreover, exogenous perturbations at the output of the DCO will be rejected.

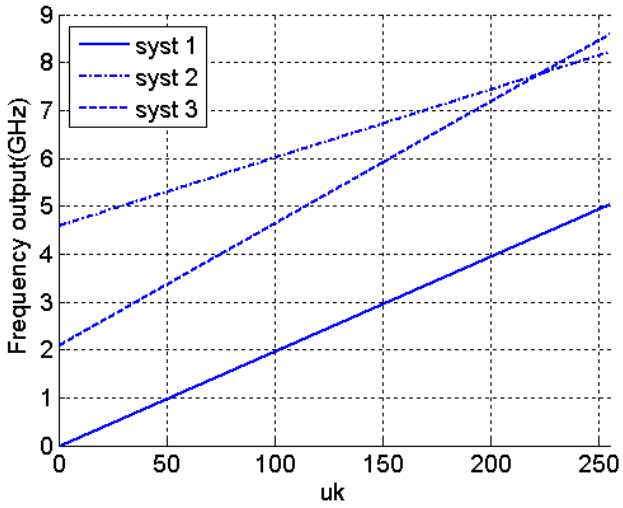

Figure 9. Variation of the characteristic curves.

Figure 10 shows the closed-loop response of ”syst 1”, “syst 2” and “syst 3” to a change in the *Set_point*. Note that the offset and the gain of the DCO change, which can happen due to PVT variability. These tests show that the equilibrium point is robust with respect to the uncertainty in the characteristic curve. Note that the response time at 5% is achieved before the 7th sampling time.

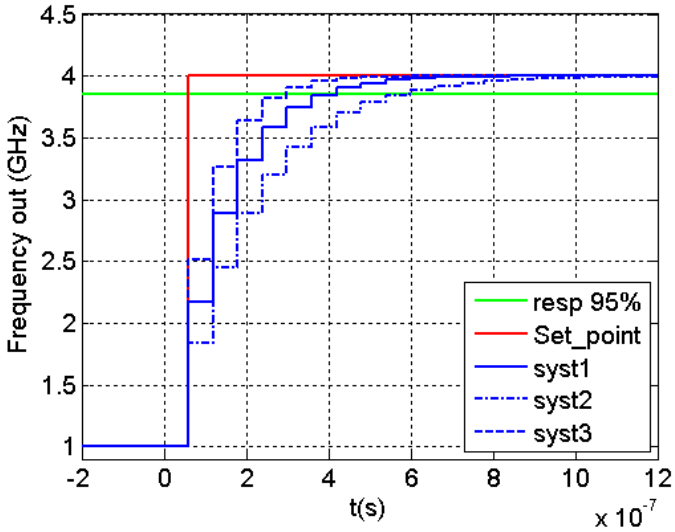

Figure 10. Evolution of the output frequency for three different systems (blue), set point (red) and response time at 5% (green).

Figure 11 shows the frequency output, when the characteristic curve changes (“syst 1”, “syst 2” and “syst 3” respectively) and when there is some exogenous perturbations at the output of the system. This example shows the robustness of the system when the optimal robust control tuning is employed.

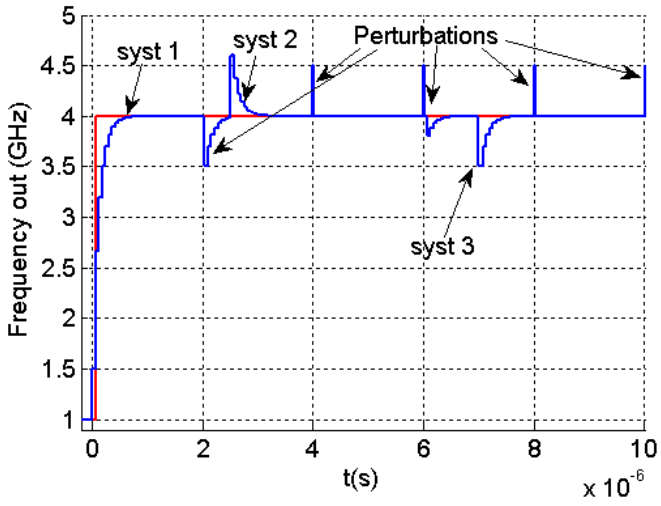

Figure 11. Evolution of the output frequency with perturbation and for three different systems.

6.3 RTL implementation

Following the various steps of the design and verification flow discussed above, the DFLL control developed in the present paper has been implemented in RTL. It must be stated that the DFLL together with its controller is fully compatible with standard cell methodology. Figure 12 shows the DFLL layout. This layout was implemented in a 32 nm technology. With a total area of 0.0016 mm² for the whole DFLL (0.000264 mm² for the DCO and 0.001336 mm² for the controller in standard cells) it is 4 to 20 times smaller than classical PLLs in the same technology. The small area overhead enables easy integration in each VFI of a GALS SoC, allowing fine-grain DVFS when combined with voltage actuators.

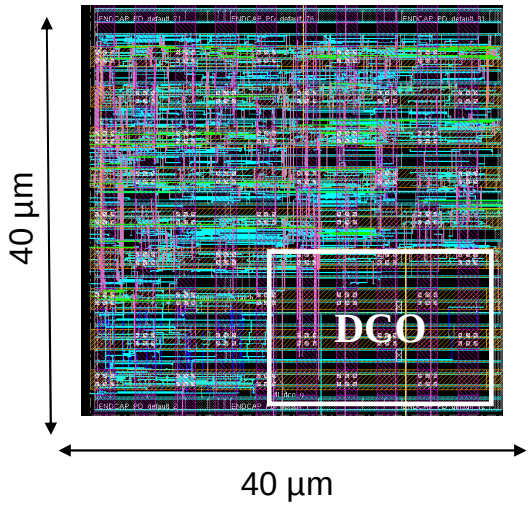

Figure 12. DFLL layout.

Figure 13 shows the signal evolutions of the VHDL RTL simulations for “syst 1”. Note that the Set_point is synchronized when getting into the closed-loop system in order to avoid an impact on the DFLL stability. The delay presented by the sensor is seen in *sensor_value*. These results match the ones obtained in the Matlab/Simulink environment, represented in Figure 10.

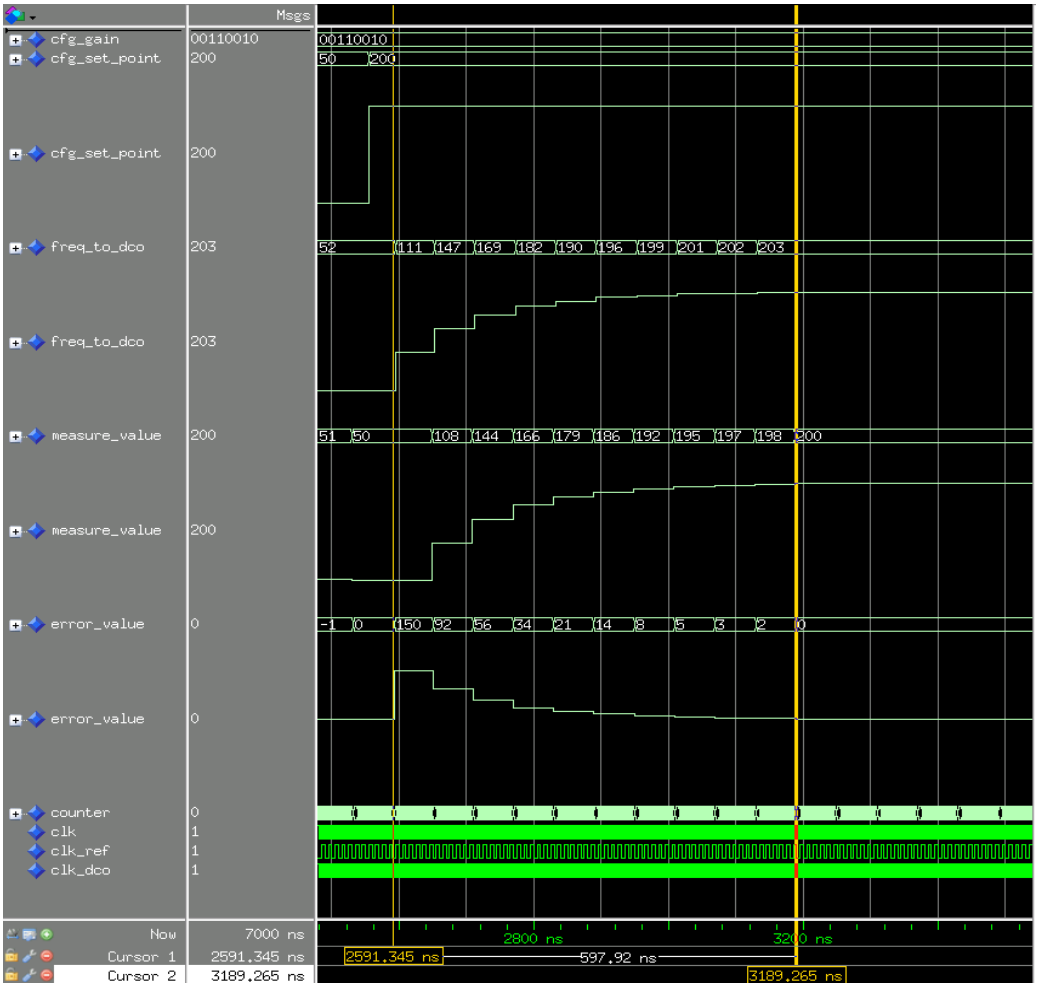

Figure 13. RTL simulation of syst 1.

7 CONCLUSION

In this paper, a small-area Digital Frequency-Locked Loop (DFLL) engine is employed to implement DVFS in GALS architecture. The use of a simple controller has allowed a fully digital implementation in standard cells, attaining a small area. Implemented in 32 nm technology, the design proposed represents 0.0016 mm^2, i.e. from 4 to 20 times smaller than classical techniques used such as Phase-Locked Loop (PLL) in the same technology. Likewise, this controller is optimal with respect to system performance (short transient response and no overshoot) and perturbation attenuation. Another suited property offered by the controller is the robustness with respect to PVT variations.

Moreover, the closed-loop system stability is guaranteed whatever the characteristic of the DCO is in a given range. Some simulations under Matlab/Simulink show the closed-loop system robustness. The DFLL with its controller was implemented in RTL in order to obtain the implementation layout.

The first version of the DFLL (included the controller proposed in this paper) has been implemented in 32 nm technology. The circuit is currently under foundery and performances attained on the real chip will be included in the final paper.

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